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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,955	03/31/2004	Jin Jeon	8054-4 CON (LW7020US-1/KY	7235

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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/814,955	JEON, JIN
	Examiner	Art Unit
	Thoi V. Duong	2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-30* is/are allowed.

6)☒ Claim(s) *31 and 32* is/are rejected.

7)☒ Claim(s) *33-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/051,701.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Amendment, Paper No. 8, filed August 26, 2002.

Accordingly, claims 10, 23, 31 and 34 were amended. Currently, claims 1-35 are pending in this application.

Terminal Disclaimer

2. The terminal disclaimer filed on March 14, 2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of USPN 6,738,109 B2 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Objections

3. Claim 12 is objected to because of the following informalities: claim 12 recites the limitation "the data electrode" in line 1. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

4. Claim 28 is objected to because of the following informalities: claim 28 recites the limitation "the source electrode" in line 7. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 31 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (USPN 6,261,881 B1).

As shown in Fig. 3, Yamazaki et al. discloses a substrate 100 comprising:

a gate pattern 102 formed on a pixel region (comprising pixel matrix circuit) and a peripheral region (comprising CMOS circuit), the pixel region and the peripheral region being disposed on the substrate 100 (see also Fig. 1A);

an active pattern 104 insulated from the gate pattern to be formed on the gate pattern 102 (see also Fig. 1B), the active pattern including a semiconductor layer (col. 4, lines 36-42);

a data pattern (118-122) electrically connected to a portion of the active pattern; and

a first insulating interlayer 123 formed on the data pattern, wherein the pixel region includes a plurality of pixels and the active pattern is comprised of amorphous silicon (col. 4, lines 36-42),

wherein, re claim 32, the pixels respectively includes a first transistor, and the peripheral regions includes a plurality of driver transistors (CMOS circuit) for driving the first transistor of the pixels (col. 13, line 52 through col. 14, line 17).

Allowable Subject Matter

7. Claims 33-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claim 33, none of the prior art of record discloses, in combination with other limitations as claimed, a substrate comprising the data pattern including a data electrode, the first insulating interlayer having a first contact hole for partially exposing the data electode of the data pattern, a second contact hole for exposing a gate electrode of a first drive transistor of the peripheral region, and a third contact hole for exposing a data electrode of a second drive transistor of the peripheral region, and the substrate further includes an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern in contact with a data electrode of the pixel region through the first contact hole, and a second electrode pattem connecting the partially exposed gate electrode of the first drive transistor with the exposed data electode of the second drive transistor through the second and third contact holes.

The most relevant references, USPN 6,261,881 B1 (US'881) and USPN 6,384,818 B1 (US'818) of Yamazaki et al., fail to disclose or suggest such combination.

As shown in Figs. 3 and 4, the US'881 discloses a reverse-stagger type TFT CMOS circuit comprising a first drive transistor (P-channel TFT) and a second drive transistor (N-channel TFT) of the peripheral region having contact holes in the insulating interlayer 117 for exposing the source and drain electrodes only. Meanwhile, the US'818 shows in Fig. 8A a CMOS circuit comprising a first drive transistor having a second contact hole for exposing the gate electrode of the first drive transistor and a second drive transistor having a third contact hole for exposing the second electrode of the second drive transistor. However, this circuit is not a reverse-stagger type TFT.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Claims 1-30 are allowed since a terminal disclaimer was filed on March 14, 2005 to overcome a nonstatutory double patenting rejection over claims 1-26 of USPN 6,738,109.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

05/19/2005

DUNG T. NGUYEN
PRIMARY EXAMINER